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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,455	12/03/2004	Michel Puech	Q84452	2876

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
OLSEN, ALLAN W	

ART UNIT	PAPER NUMBER
1792	

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05/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/516,455	PUECH, MICHEL	
	Examiner	Art Unit	
	Allan Olsen	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,456,796 issued to Gupta et al. (hereinafter, Gupta).

Gupta teaches ramping up the power level in a plasma reactor (abstract; Figure 2b; column 3, lines 6-38column 2, lines 44-45).

Gupta teaches a plasma etching method wherein a gas that is inert for the substrate is injected into the reaction chamber and the power of the plasma excitation electromagnetic wave is raised progressively until the appropriate nominal power is reached, thereby forming an inert gas plasma, which would progressively heat up the plasma chamber's leakproof wall of dielectric material. Gupta teaches injecting a reactive gas into the reaction chamber to replace the inert gas and to perform etching by the plasma of the active gas. Note the following excerpt from column 5:

> Thus, it is preferred when practicing this embodiment of the present invention for these applications to initiate and slowly ramp the plasma power level in the presence of an inert gas, such as Argon. In this way contaminants are not agitated by the plasma ramp and contamination is minimized, as taught above. When the plasma is at its full power level (indicated by numeric designator **23** on FIG. **2***b*), the flow of inert gas to the reaction chamber may be stopped and the desired reactant gas is introduced into the chamber.

Gupta does not explicitly teach an inductively coupled plasma process wherein the substrate is biased.

It would have been obvious to one skilled in the art at the time the invention was made to carry out Gupta's method in an inductively-coupled plasma apparatus while biasing the substrate because Gupta states, in column 2:

> The present invention has application in any plasma tool, such as those that are used in deposition, etching, or in-situ dry clean processes on a chemical vapor deposition ("CVD"), etch, or physical vapor deposition ("PVD") system.

And in column 4:

> Thus, specific details of reaction chamber construction and electrode arrangement therein; actual RF signal generation and control, and plasma frequency/power levels are either considered well known or a matter of choice.
>
> ⋮
>
> It is expected that the present invention will find broad application in any process chamber employing a plasma as part of a process step.

Furthermore, the examiner takes Official Notice that the biasing of the substrate during an inductively coupled plasma process is an extremely common mode of plasma processing. Therefore, in view of the above noted teachings of Gupta, it is likely that the skilled artisan would immediately envisage the claimed mode of plasma processing.

Gupta does not teach progressively increasing the plasma excitation power in a manner to ensure that the thermal shock applied to the leakproof wall remains below a wall-destroying threshold.

It would have been obvious to one skilled in the art, at the time the invention was made, to operate the plasma apparatus in a manner that would not destroy the apparatus.

Gupta does not teach progressively establishing the plasma excitation power at the beginning of a reaction chamber's operation following a period of inactivity. And, Gupta does not teach the plasma process comprises a succession of etching periods that use fluorine-containing gas and passivation periods that use an etching passivation gas.

It would have been obvious to one skilled in the art, at the time the invention was made, to use Gupta's method when initiating the plasma for any plasma process, including one at the beginning of a reaction chamber's operation, following a period of inactivity, and including a plasma process that comprises a succession of etching periods that use fluorine-containing gas and passivation periods that use an etching passivation gas because the benefit of reducing or eliminating wafer contamination by avoiding stirring up and circulating particles within the reaction chamber (column 3, lines 6-15) would be realized during any plasma start-up, including a plasma process that takes place following a period of inactivity and including a plasma process that comprises a succession of etching periods, which use a fluorine-containing gas, and passivation periods that use an etching passivation gas. The examiner takes Official notice that the Bosch process, which is a well-known and widely used plasma processing technique, comprising a succession of etching periods, using a fluorine-containing gas, and passivation periods using an etching passivation gas.

Response to Arguments

Applicant's arguments filed February 15, 2008 have been fully considered but they are not persuasive. Applicant argues:

> *Claim 1 recites, in part, "biasing the substrate." The Examiner acknowledges that Gupta fails to disclose this aspect of claim 1, but indicates that biasing a substrate is an extremely common mode of plasma processing.*

In response, the examiner notes that applicant's characterization of the examiner's position is not quite correct. The examiner did acknowledge that Gupta fails to disclose biasing the substrate. To the contrary, as noted below, Gupta does teach biasing the substrate. The Office action stated (with emphasis added) that "Gupta does not explicitly teach an inductively coupled plasma process wherein the substrate is biased", that is to say, Gupta does not teach the biasing of the substrate in conjunction with an ICP. Throughout the specification, Gupta teaches supplying RF energy to the substrate (i.e., biasing). See, for example, the following excerpt from column 1. Also, see, column 3, lines 6-7 and 66-67; and column 4, lines 7-13.

> A plasma is often used during the fabrication of integrated circuits in a reaction chamber to excite individual atoms of chemical reactants within the chamber. A typical reaction chamber **10** (represented schematically in FIG. 1) confines the reactants used during semiconductor wafer **14** processing. The semiconductor wafer **14** is electrically coupled to a cathode **13**, and a plasma is initiated within the reaction chamber when an RF signal is generated at a generating source **11** and coupled from the source **11** to an anode **12** and the cathode **13** by a control and coupling circuit **15**.

Applicant argues:

> *The Examiner offers no evidence that it would be obvious for one of ordinary skill in the art to bias the substrate disclosed in Gupta.*

And,

> *"one of ordinary skill in the art would not bias the wafer noted in Gupta, as biasing the substrate would likely increase the risk that contaminants would be attracted to the substrate along with the plasma".*

In response, the examiner notes that Gupta's explicit teaching with respect to the biasing of the substrate provides ample evidence that biasing would be obvious conducting the process in an ICP reactor, especially in view of Gupta's teaching in column 4 that the process may be used in "any process chamber employing a plasma".

> Thus, specific details of reaction chamber construction and electrode arrangement therein; actual RF signal generation and control, and plasma frequency/power levels are either considered well known or a matter of choice.
>
> ⋮
>
> It is expected that the present invention will find broad application in any process chamber employing a plasma as part of a process step.

Applicant also argues:

The Examiner simply notes that "it is likely that the skilled artisan would immediately envisage the claimed mode of plasma processing." However, the Examiner has not provided any support for this conclusion. Simply because an element is known in the art does not indicate that the element may be combined with a separate reference.

In response, the examiner notes that there are very few types of plasma reaction chambers, and inductively coupled reactors represent one of the most widely used type of reactors. An ICP reactor can be operated without or without substrate biasing - most frequently, the substrate is biased. As such, the examiner maintains that, as a result of Gupta teaching that "any process chamber can be used" and that "actual RF signal generation and control … are well known or a matter of choice", one skilled in the art would immediately envisage, as if Gupta had explicitly taught, applying the method in an ICP reactor while biasing the substrate.

Lastly, regarding applicant's argument that “one of ordinary skill in the art would not bias the wafer noted in Gupta, as biasing the substrate would likely increase the risk that contaminants would be attracted to the substrate along with the plasma”, the examiner notes that this argument is directly counter to Gupta’s explicit teaching of substrate biasing.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allan Olsen whose telephone number is 571-272-1441. The examiner can normally be reached on M, W and F: 1-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Allan Olsen/